**Intel 80386 and subsequent architecture combining segmentation and two-level paging**

**logical address**

- selector
- offset

- descriptor table (segment table)
- base
- limit
- segment descriptor

- offset < limit

- segmentation fault

**linear address**

- base
- offset

- directory
- page
- offset

- TLB
  - Translation look-aside buffer (cache)

- MPTBR
  - (master page table base register, called by Intel the **page directory base register**)

- directory entry (PTBR)

- page-table entry (frame)

- page table (inner page table)

- page directory (outer page table)

**KEY**

- bold words: Intel terms
- bold boxes: on CPU, not RAM

* 12 bits = 0..8191, giving Windows XP a page size of 8192 = 2^13

** "Linear" means what the physical address would be if there were no paging.

Page faulting is not shown, nor are dirty and valid bits