Operating Systems Day 2 Study Questions

1. One of the themes in our course is parallelism. In what way does DMA illustrate parallelism? [easy; p. 35] In what way is DMA unable to be fully parallel with a user program that accesses RAM? [harder; “cycle stealing,” pp. 35–36]

2. What is memory-mapped i/o? [p. 37]

3. Disk access time = seek time + rotational latency time. Which do you think is the slower of the two times? [p. 38]

4. What is the problem of cache consistency? [“coherency,” p. 43; in Chapter 16, a solution to cache consistency will be proposed.] Why not solve it by making the cache as large as a disk? [Question 2.9, p. 56]

5. [Question 2.5, p. 55]

6. Do you think that the range checking implied by Figure 2.10 on p. 49 should be calculations done by the CPU or by logic wired into dedicated hardware? Why or why not?

7. Why do you think that time slices that are too big are bad, and time slices that are too small are bad? Use the term “context switching” in your answer. [pp. 49–50; we will revisit this question a few time]