

Study Questions for Patterson & Hennessy
Chapter 4 and two small parts of Chapter 5 beyond p. 315

This study guide is again in the form of questions.

1. Which of the three factors of this master equation relate to the hardware and instruction set architecture?

$$executionTime = \frac{time}{processes} = \left(\frac{instructions}{processes} \right) \times \left(\frac{cycles}{instructions} \right) \times \left(\frac{time}{cycles} \right) (*)$$

2. Doubling the speed (GHz) of a processor does not double the speed of the computer because _____. (Don't just say "Amdahl's law." Explain.)

3. The performance of a computer for a give application is defined as 1/T, where T is
- Total execution time, application program time plus operating system time on the application's behalf, including input/output.
 - The application program execution time excluding any operating system time like input/output on the program's behalf.
 - Operating system execution time including input/output on behalf of the application.
 - Total execution time less the time spent in input/output.

[The performance of a **computer** for a given application is (a), including i/o time, and it must take into account the speed of components other than the CPU. I mentioned the bus in class as an example of such a component. The caption of Figure 4.5 on p. 260 offers this disclaimer: "SPEC CPU benchmarks measure wall clock, but because there is little i/o, they measure CPU performance." So the graphs on p. 261 are approximations to CPU performance. If the question said the "performance of the **CPU**," the answer would be that T is the execution (CPU) time, both in and out of the kernel. Recall that when you write programs in MIPS, for example, you call on the kernel to do some of your work via a syscall.]

4. (True or false) A computer that is fastest for playing chess is sure to be fastest for calculating how proteins fold. [Note that I didn't say "is likely to be fastest."]

5. Benchmarks are more useful in measuring performance than processor speed in GHz or "native MIPS" rate because _____.

6. A MIPS instruction on a real MIPS machine executes in five steps, three of which do not depend on which instruction it is. What are those three steps? What are the remaining two steps? Which of the remaining steps is executed by each of these instructions: ADD, BEQ, LW, SW?

7. Which instruction is likely to take longer: LW or SW?

8. Circle the true statements about MIPS architecture with multicycle data path (the 5-CPI model) as contrasted with the 1-CPI model:

- Five extra registers are needed: IF, MEM, A, B, and ALUout.
- Only one RAM unit is needed, because it now can be used for both instructions and data.
- All additions can now be done by a single ALU.
- An extra Mux with an extra IorD control wire is needed.

[I cheated here by including two things that begin Monday's lecture. All are true, but only (a) and (b) were covered on Friday. You can look at Figure 5.28 on Page 323 to see that (c) and (d) are also true.]

9. Computational problem: See end of Chapter 4, questions: 4.1, 4.2, 4.8, and 4.9.