

RISC vs. CISC

	RISC (like MIPS)*	CISC (like Intel)
registers	many	few
addressing modes	few (R, I, J)	many
control	hardwired	microcoded
pipelining	extensive	limited
length of instructions	fixed	variable
complexity	in the compiler of high level code	in the microcode
memory access	load and store instructions only	many instructions
registers per instruction	up to three	up to two
parameter passing through ...	on-chip register set “register window”	off-chip memory (e.g. stack)
instruction timing	single cycle except load, store	multiple cycle

* MIPS chips are found in Silicon Graphics workstations, Cisco routers, and Sony and Nintendo game consoles. MIPS originally stood for Microprocessor without Interlocked Pipeline Stages.

I have shaded aspects of the contrast which we did not concentrate on in our course.

Some information for this chart was found in Linda Null and Julia Lobur's book, *The Essentials of Computer Organization and Architecture*. Jones and Bartlett, 2003, p. 418.